REMARKS

With respect to Japan 64-61953 which, according to the Examiner, was not enclosed with the Information Disclosure Statement dated August 22, 2000, submitted herewith is a copy of this reference. It should be noted that the return card (copy enclosed) that accompanied the Information Disclosure Statement dated August 22, 2000 and date stamped by the USPTO sets forth "(7) refs" which is the number of references that are listed in this Information Disclosure Statement and there is no indication that the number of any of the seven references received by the USPTO is different from the reference numbers listed on Form 1449 of the Information Disclosure Statement.

Figures 8A, 8B, and 9 have been amended as required by the Examiner, so the objection to the drawings, set forth in Paragraph 1 of the Office Action, is overcome.

Applicant acknowledges with appreciation the prospective allowance of claims 7 and 8, subject to overcoming the objections to these two claims set out in Paragraph 2 of the Office Action. The Examiner has objected to claims 7 and 8 on "informalities." The Examiner contends that claims 7 and 8 should further recite "while the potential of said shield electrode is made to be equal to that of the substrate." The Examiner has not set out any reason for requiring this amendment and Applicant cannot identify any apparent need for making this amendment. The Examiner is requested to provide the reason why such an amendment is believed to be necessary if the requirement to make this amendment is repeated.

With respect to the objection to the specification, the specification, at page 10, lines 16 and 17, reads:

"For example, the drain region includes a p-type conductive layer"

which is the limitation added by claim 10. Applicant respectfully requests withdrawal of the objection to the specification.

Reconsideration and allowance of claims 1 and 5, "rejected under 35 U.S.C. 102(b) as being anticipated by Kuriyama et al. (5,550,435)," are respectfully requested.

The Examiner contends that Kuriyama et al. discloses a drain region having a first well (6) of n+ impurity concentration and a second well (4) of n impurity concentration. Claim 1, as amended, specifies additional details about these two wells, namely that one of the two wells making up the drain region is provided around a circumference of the other of the two wells making up the drain region. As amended, claim 1 reads

> "one well having a low impurity concentration is provided around a circumference of the other well having a higher impurity concentration" (emphasis added)

Support for the amendment of claim 1 can be found, for example, at page 21, lines 9-13, of the present specification. This structure is neither taught nor suggested by Kuriyama et al. Rather, Kuriyama et al. shows, for example in Figure 3, that both well regions are provided side-by-side, with neither of the wells surrounding the other of the wells.

With respect to rejection of claim 5, this claim has been amended to specify:

> "the drain region including at least two wells having different impurity concentrations, a first of the at least two wells being provided around a circumference of the second of the at least two wells"

Thus, claim 5, as amended, is similar to claim 1, as amended. With the structure defined by claim 5, as amended, neither disclosed nor suggested by Kuriyama et al., Applicant's invention, as defined by claim 5, is different from Kuriyama et al.

Reconsideration and allowance of claims 2 and 3, rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (5,550,435), in view of Akamatsu et al. (5,396,096)," are respectfully requested. Akamatsu et al. has been

applied against claims 2 and 3, which are dependent upon claim 1, because the Examiner believes that the limitations added by claims 2 and 3 are disclosed by this reference. Whether or not this is so is academic because Akamatsu et al. fails to make up for the deficiency of Kuriyama et al., as applied against claim 1, so claims 2 and 3, dependent on claim 1, distinguish Applicant's invention, as defined by claims 2 and 3, from the combination of Kuriyama et al. and Akamatsu et al.

Reconsideration and allowance of claim 4, rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (5,550,435), in view of Ogata (JP360022375A)," are respectfully requested.

The Examiner has applied Kuriyama et al., in the rejection of claim 4, in much the same manner as with the rejection of claim 1. The Examiner, however, acknowledges that Kuriyama et al. fails to disclose that

> "the gate electrode of the field effect transistor portion has a shape including portions having at least two different gate widths"
>
> and
>
> "a part of the gate electrode is provided in such a manner as to cover an end of the drain region"

To make up for this deficiency of Kuriyama et al., the Examiner has applied Ogata in combination with Kuriyama et al. in the rejection of claim 4. The Examiner's position is that "a gate widening near the drain end of the channel so as to increase withstand voltage has long been known in the art, as evidenced by Japanese Patent to Ogata."

As described at page 29, line 9 through page 30, line 21 of the present specification, in the present invention, a portion of the gate electrode nearer the drain region is provided with a larger width a portion of the gate electrode nearer the source region. Referring to Figure 2 of Ogata, a "Y" shaped gate electrode (12) is provided such that one end of the gate electrode splits into two branches. This is different from the present invention.

Ogata fails to disclose or suggest a gate electrode having a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of the source electrode nearer the source region. Rather, because Ogata discloses branching the gate electrode into two smaller branches to obtain a "Y" shape, the total width of the gate electrode nearer the drain region would appear to be identical to the total width of the gate electrode at the source end.

Claim 4 has been amended to recite

> "the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of the source electrode nearer the source region" (emphasis added)

Thus, Applicant's invention, as defined by amended claim 4, is different from the combination of Kuriyama et al. and Ogata.

Reconsideration and allowance of claims 6, 9, and 11 through 13, rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (5,550,435) in view of Japanese Patent to Hirano et al. (JP409063467A)," are respectfully requested.

Hirano et al. has been applied against claim 6, which is dependent upon claim 5, because the Examiner believes that the limitations added by claim 6 are disclosed by this reference. Whether or not this is so is academic because Hirano et al. fails to make up for the deficiency of Kuriyama et al., as applied against claim 5, so claim 6, dependent on claim 5, distinguishes Applicant's invention, as defined by claim 6, from the combination of Kuriyama et al. and Hirano et al.

With respect to the rejection of claim 9, the Examiner first states that Kuriyama et al. discloses all of "the limitations of claim 9 up to and including line 18" and then states that "Kuriyama et al. do not specifically teach the limitation concerning the drain (lines 15-18)." Given the references to Hirano et al. by the

Examiner, Applicant will treat the Examiner's comments about the specific teachings of Kuriyama et al. as applying to lines 1 through 14 of claim 9.

The Examiner refers to Figure 5 of Hirano which the Examiner contends discloses the claimed symmetrical arrangement of the gate electrode with respect to the cathode of the electron emission source. Applicant believes that the Examiner is referring to elements 43 and 47, as shown in Figure 5 of Hirano et al. as supposedly teaching the claimed arrangement of the gate electrode with respect to the electron emission source. If so, this is incorrect because neither element 43 nor 47 of Hirano et al. are gate electrodes and for that reason, Hirano et al. does not disclose gate electrodes positioned symmetrical in a plane with respect to the cathode portion of the field emission electron source portion, as specified by claim 9. Consequently, Applicant's invention, as defined by claim 9, is different from the combination of Kuriyama et al and Hirano et al., whether or not it would be obvious to combine these two references. Applicant does not concede that it would be obvious to combine these two references.

Reconsideration and allowance of claim 10, rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. and Hirano et al. as applied to claim 9 above, and further in view of Bergonzoni (4,968,639)," are respectfully requested. Bergonzoni has been applied in the rejection of claim 10 because the Examiner contends that

> "the inclusion of p-type conductive layers in an n-type drain has long been known by those skilled in the art of lightly-doped drain type field effect transistors as a means to combat punch-through, as witnessed by Bergonzoni, who teaches p-type layers 13' in n-type drain and source regions 31 (cf. column 2, lines 45-63)"

Whether or not this is so is academic because Bergonzoni fails to make up for the deficiency of the combination of Kuriyama et al. and Hirano et al., as applied against claim 9, so claim 10, dependent on claim 9, distinguishes Applicant's invention, as defined by claim 10, from the combination of Kuriyama et al., Hirano et al. and Bergonzoni. Consequently, Applicant's invention, as defined by claim 9, is different from the combination of Kuriyama et al, Hirano et

al., and Bergonzoni whether or not it would be obvious to combine these three references. Applicant does not concede that it would be obvious to combine these three references.

Newly added claims 14 through 17 are, respectively, dependent upon claims 1, 4, 5 and 7 and each recite that the extraction electrode is provided in a region above the drain region and away from an interface between regions of different impurity concentrations. This is clearly shown in the Figures 1 through 4 of Applicant's drawings, for example. Providing the extraction electrode in a region that is not above an interface between regions of different impurities (for example, above the interface between elements 3 and 4 of Figure 1 of Applicant's drawings) reduces the chance of hot-electrons affecting the potential of the extraction electrode and thereby affect the output of the electron emission source.

Kuriyama, in contrast, discloses a large grid electrode provided in a region that is above the n+ well (6) and the n well (4) and, as such, is more prone to being affected by hot-electrons.

In view of the foregoing amendments and remarks, this application is in condition for allowance which action is respectfully requested.

Respectfully Submitted,

Andrew L. Ney, Reg. No. 20,300
Attorney for Applicant

ALN/ap
Enclosures:
Version with markings to show changes made
Figures 8A, 8B and 9 marked with red corrections
Copy of Post Card dated August 22, 2000
Copy of reference 64-61953
Dated: August 13, 2002

P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. 18-0350 of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on:

8/13/02

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS:

1. (As Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via an insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion;

the drain region includes different impurity elements and includes at least two wells having different impurity concentrations having symmetrical impurity distributions; and

of the at least two wells, one well having a low impurity concentration is provided around a circumference of the other well having a higher impurity concentration [at an end of the drain region which contacts a channel region of the field effect transistor portion].

4. (As Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via an insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion;

the gate electrode of the field effect transistor portion has a shape [including portions having at least two different gate widths] such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of the source electrode nearer the source region; and a part of the gate electrode is provided in such a manner as to cover an end of the drain region.

5. (As Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via a first insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion;

the drain region including at least two wells having different impurity concentrations, a first of the at least two wells being provided around a circumference of the second of the at least two wells;

a gate insulating film is provided between the gate electrode of the field effect transistor and the p-type silicon substrate; the gate insulating film includes a film thinner than the first insulating film, the first insulating film being provided between the extraction electrode and the p-type silicon substrate; and the gate insulating film is buried with the first insulating film.

Claims 14-17 are newly added.